Physical AI

EventBelt – Event-Cameras and Neuromorphic Computing for Real-Time Intelligent Manufacturing

Pro²Future

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MOTIVATION & GOALS

Deploying AI provides significant operational benefits, but the associated energy costs must remain as low as possible to achieve **long-term sustainability in intelligent manufacturing**.

In the EventBelt project, we strive for **real-time material identification** while utilizing energy-efficient processing mechanisms. The prototype combines an event camera with a **Recurrent Spiking Neural Network** (RSNN) architecture deployed directly on low-power edge hardware.

By processing **event-driven sparse data**, this approach minimizes computational overhead while maintaining high sorting accuracy for sustainable circular economy applications.

Project FactBox

Project Name EventBelt
Project ID Praktika für Studentinnen 2026
Duration 1 Month

Area 1
Area Perception

Project Lead
Dr. Michael Haslgrübler

APPROACH

The project started with **conveyor belt setup** and subsequent **data collection** & dataset assembly, where asynchronous event streams are systematically captured using an event camera mounted above a miniature conveyor belt to **record** diverse motion passes **under varying speeds**.

During **RSNN** Training & Hyperparameter Optimization, a Recurrent Spiking Neural Network (RSNN) architecture utilizing **residual Leaky Integrate-and-Fire (LIF)** blocks is trained, using a **surrogate gradient approach**. Finally, everything was integrated and deployed on a Raspberry Pi where it provides seemingly **instantaneous classification**.

CONTRIBUTION

Scientific contribution

- Energy-Efficient temporal event processing .
- millisecond real-time material recognition
- empirical benchmark for deploying green AI solutions

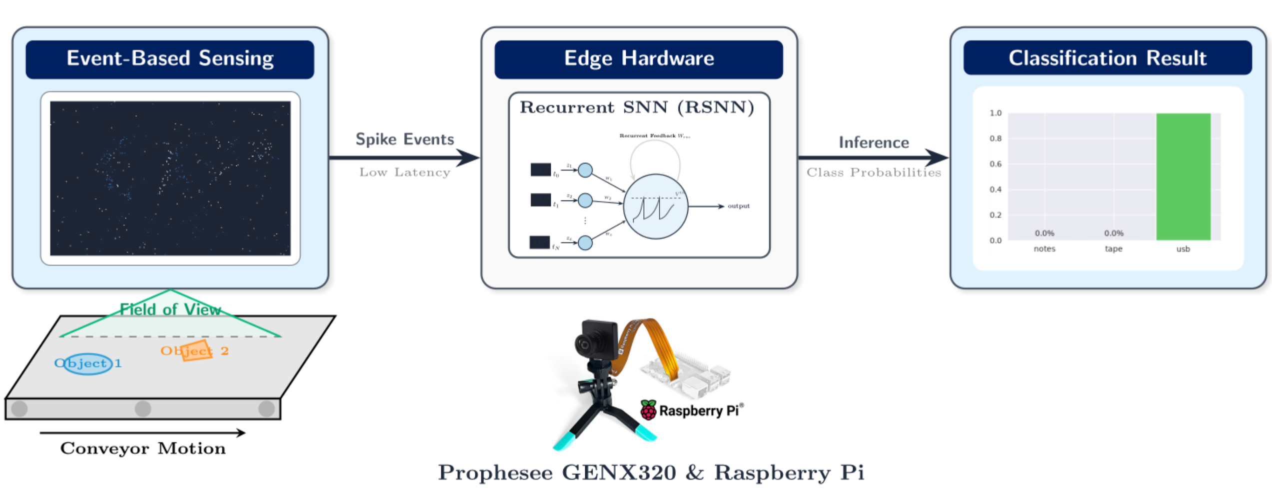
Economic contribution

- Real-Time Conveyor Belt Sorting
- Decreases Edge Hardware Unit Costs
- Lower Latency in Processing Signal

Layer / Stage	Configuration	Output Channels
Input	48×48, 2 channels (polarity)	2
Initial convolution	7×7 kernel, stride 1, padding 1	64
Residual stage 1	2 blocks, LIF, 3×3 kernel, stride 1	64
Residual stage 2	2 blocks, LIF, 3×3 kernel, stride 2	128
Residual stage 3	2 blocks, LIF, 3×3 kernel, stride 2	256
Pooling	Global average pooling	256
Output layer	Fully connected	`num_classes` (3)

RSNN Internal Configuration

SYSTEM ARCHITECTURE



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